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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,235	04/24/2001	Aaron Hal Dinwiddie	RCA-89210	4995

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,235	DINWIDDIE ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

memory unit for storing a computer code that is downloaded from the memory unit of the memory card (see col. 8, lines 40-57). The reference also teaches a card interface having a first data port and a second data port for transferring data in accordance with a first ~~second~~ & second standard (see Figures 9-11; col. 5, lines 10-22; "mother card" and "daughter card"). The cited reference also teaches a microcontroller coupled to the card interface and to the memory (see Figure 3, "40") for, if said card is a memory card, reading said computer code from said memory card by way of said second data port to said memory, for thereby updating the computer code stored in said memory so as to effect a change of the functional operation of the apparatus (see col. 4, lines 55-58).

As for claim 5, Harari et al. teaches means for producing a first signal coupled to an integrated circuit card connection and means for analyzing a second signal produced by a memory card in response to the first signal (see col. 8, lines 40-57).

As for claim 6, Harari et al. teaches integrated circuit cards that are not memory cards do not produce a cited signal (see "type field", col. 13, lines 56-58).

As for claim 9, Harari et al. teaches transferring computer code from the memory card to a computer controlled device memory unit (see col. 8, lines 53-57).

Considering claim 10, Harari et al. teaches means for accepting or rejecting the computer code for transference from the memory card to a computer controlled device memory unit (see "type field", col. 13, lines 56-58).

Regarding claim 11, Harari et al. teaches the apparatus for loading computer code from a memory type integrated circuit card preloaded with a computer code. Accordingly, the reference also teaches the limitations corresponding to the method for loading computer code in a computer-controlled device having a smart card interface for receiving a smart card. The present claim is rejected under the same basis.

As for claim 12, Harari et al. teaches a method including applying a first signal coupled to a memory card connection and analyzing a second signal produced by a memory card in response to the first signal (see col. 8, lines 40-57). In addition, Harari et al. teaches a method capable of identifying card types (see "identifying data 220"; col. 13, lines 49-64).

5. Claims 7 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. [US 6,893,268 B1] in view of Hayes et al. [US 6,223,348].

In consideration of claim 7, Harari et al. does not teach a card interface applying a first signal to a clock signal connector of the integrated circuit card connection and receiving a second signal on a data input/output connector of the integrated circuit card connection, as claimed. As for this limitation, Hayes et al. teaches applying a signal to a clock signal connector of the

integrated circuit card connection (see col. 7, line 45) as well as receiving a second signal on a data input/output signal connector of the integrated circuit card connection (see col. 7, lines 43-44). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a device having circuit and program logic for selecting a device which is activated at a given time (see Smart Card 15 and EEPROM 27; col. 7, lines 33-38) as taught by Hayes et al.

Considering claim 14, Harari et al. does not teach the step of "analyzing a header of said computer code to determine the validity of the computer code", as claimed. As for this limitation, Hayes et al. teaches a method including the step of analyzing a header of the computer code to determine the validity of the computer code (see 6, line 64). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited references for the reasons stated above.

As for claim 15, Hayes et al. teaches toggling a reset signal (inherent, see col. 7, lines 41-47). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited references for the reasons stated above.

As for claim 16, Hayes et al. teaches monitoring a clock input signal terminal for a first signal in response to the toggled signal (inherent, see col. 7, lines 41-47). At the time of the

invention, one of ordinary skill in the art would have been motivated to combine the cited references for the reasons stated above.

As for claim 17, Hayes et al. teaches a method where a second signal is generated in response to detection of a first signal (see col. 7, lines 41-47). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited references for the reasons stated above.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. [US 6,893,268 B1] in view of Campinos et al. [US 6,266,415 B1].

As for claim 13, Harari et al. does not teach a method including activating an NRSS interface. NRSS-type cards are well known in the art. Campinos et al. teaches (see col. 1, lines 13-20) a card complying with the American NRSS standard (standing for "National Renewable Security System"). Accordingly, one of ordinary skill in the art would have been motivated to combine the references in order to have a method specifying a well known standard for cards, as taught by Campinos et al.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 5-7, and 9-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Kurihashi et al. [US 6,457,647 B1] teaches a memory card adaptor to facilitate upgrades.
- Hisano [US 6,138,173] teaches I/O expansion circuit having a plurality of selectable I/O ports.
- Charles et al. [US 6,044,215] teaches an apparatus, providing interface having first and second data ports (see Figure 1). In addition, Charles et al. teaches a controller (see col. 17, line 48). The Charles et al. reference also teaches ports in accordance with different standards (see col. 17, lines 12-19).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
12 December 2005

KIM HUYNH
PRIMARY EXAMINER